

IN THE CLAIMS:

Rewrite the pending claims as follows:

Sub O' 1. (Currently Amended) A method of assigning a buffer size in a video decoder, ~~said method comprising the steps of:~~  
 establishing a first buffer size for a scalable buffer;  
 processing a video data stream utilizing with said scalable buffer configured to said first buffer size;  
 selecting a second buffer size for said scalable buffer;  
 processing said video data stream utilizing with said scalable buffer configured to said second buffer size;  
 creating memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and the processing with said scalable buffer configured to said second buffer size; and  
 assigning a buffer size for said scalable buffer in accordance with said memory utilization data;  
wherein the memory utilization data includes cache miss rate data.

2. (Currently Amended) The method of claim 1 wherein said establishing step and said selecting step each include ~~the step of~~ defining a buffer size as a multiple of ~~an encoded image data block in the form of a~~ buffer size for storing a single macroblock.

3. (Original) The method of claim 1 wherein said processing of said video data stream includes utilizing said scalable buffer with a variable length decoder.

4. (Original) The method of claim 1 wherein said processing of said video data stream includes utilizing said scalable buffer with an inverse discrete cosine transfer function module.

5. (Original) The method of claim 1 wherein said processing of said video data stream includes utilizing said scalable buffer with a motion compensator.

6. (Currently Amended) The method of claim 1 wherein said creating ~~step~~ includes ~~the step of~~ creating cache utilization data defining data cache miss rates.
7. (Currently Amended) The method of claim 1 wherein said creating ~~step~~ includes ~~the step of~~ creating cache utilization data defining instruction cache miss rates.
8. (Currently Amended) The method of claim 1 further comprising ~~the step of~~ modifying the size of video data stream processing instructions to correspond to said buffer size selected in said assigning step.
9. (Currently Amended) The method of claim 8 wherein said ~~modifying step~~ includes ~~the step of~~ loop unrolling data stream processing instructions to correspond to said buffer size selected in said assigning step.
10. (Cancelled)
11. (Cancelled)
12. (Cancelled)
13. (Currently Amended) A computer readable memory to direct a computer to function in a specified manner, comprising:
  - a buffer management module to establish a first buffer size and a second buffer size for a scalable buffer;
  - a video decoding module to process a video stream utilizing with said scalable buffer configured to said first buffer size and then said second buffer size; and
  - an analysis module to create memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and during the processing with said scalable buffer configured to said second buffer size, said analysis module including a buffer size adjuster to assign a buffer size for said scalable buffer in accordance with said memory utilization data;
  - wherein the memory utilization data includes cache miss rate data.

*A' could*

14. (Currently Amended) The computer readable memory of claim 13 wherein said buffer management module establishes said first buffer size as a first multiple of ~~an encoded image data block~~ a buffer size for storing a single macroblock and said second buffer size as a second multiple of ~~an encoded image data block~~ a buffer size for storing a single macroblock.

15. (Cancelled)

16. (Original) The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with a variable length decoder.

17. (Original) The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with an inverse discrete cosine transfer function module.

18. (Original) The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with a motion compensator.

19. (Original) The computer readable memory of claim 13 wherein said analysis module creates cache utilization data defining data cache miss rates.

20. (Original) The computer readable memory of claim 13 wherein said analysis module creates cache utilization data defining instruction cache miss rates.

21. (New) The computer readable memory of claim 13 wherein said analysis module further includes a subsystem to modify the size of video data stream processing instructions to correspond to said buffer size assigned by the buffer size adjuster.

22. (New) The computer readable memory of claim 21 wherein said subsystem performs loop unrolling of data stream processing instructions to correspond to said buffer size assigned by the buffer size adjuster.